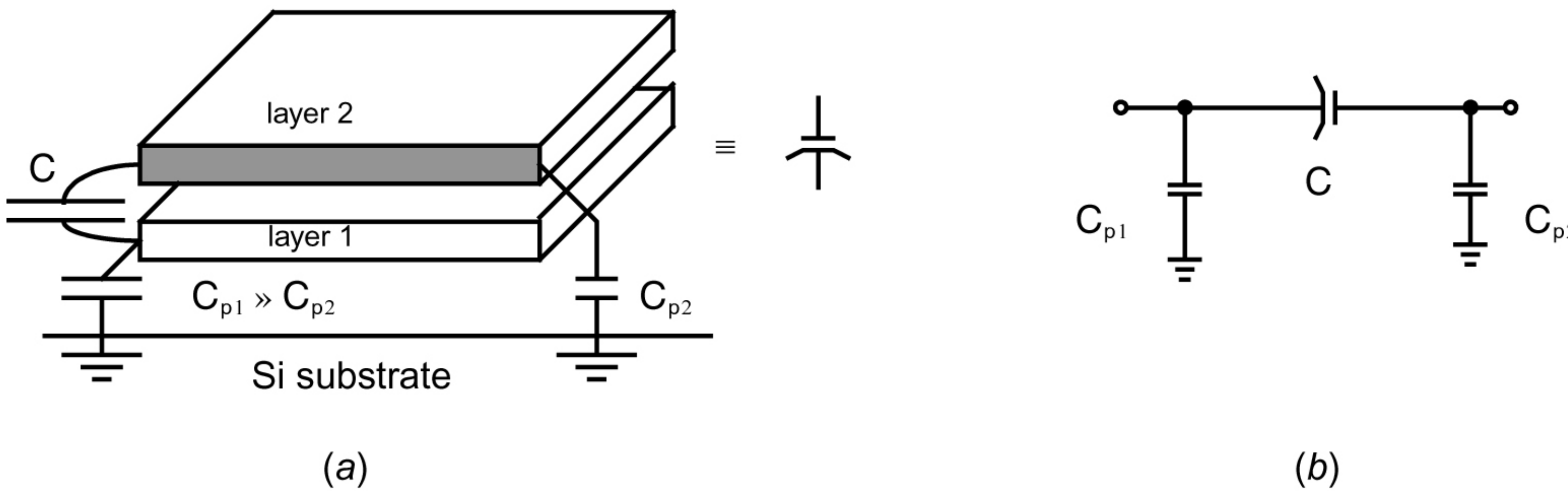
Introduction to Switched-Capacitor Circuits

Sections 14.1 & 14.2

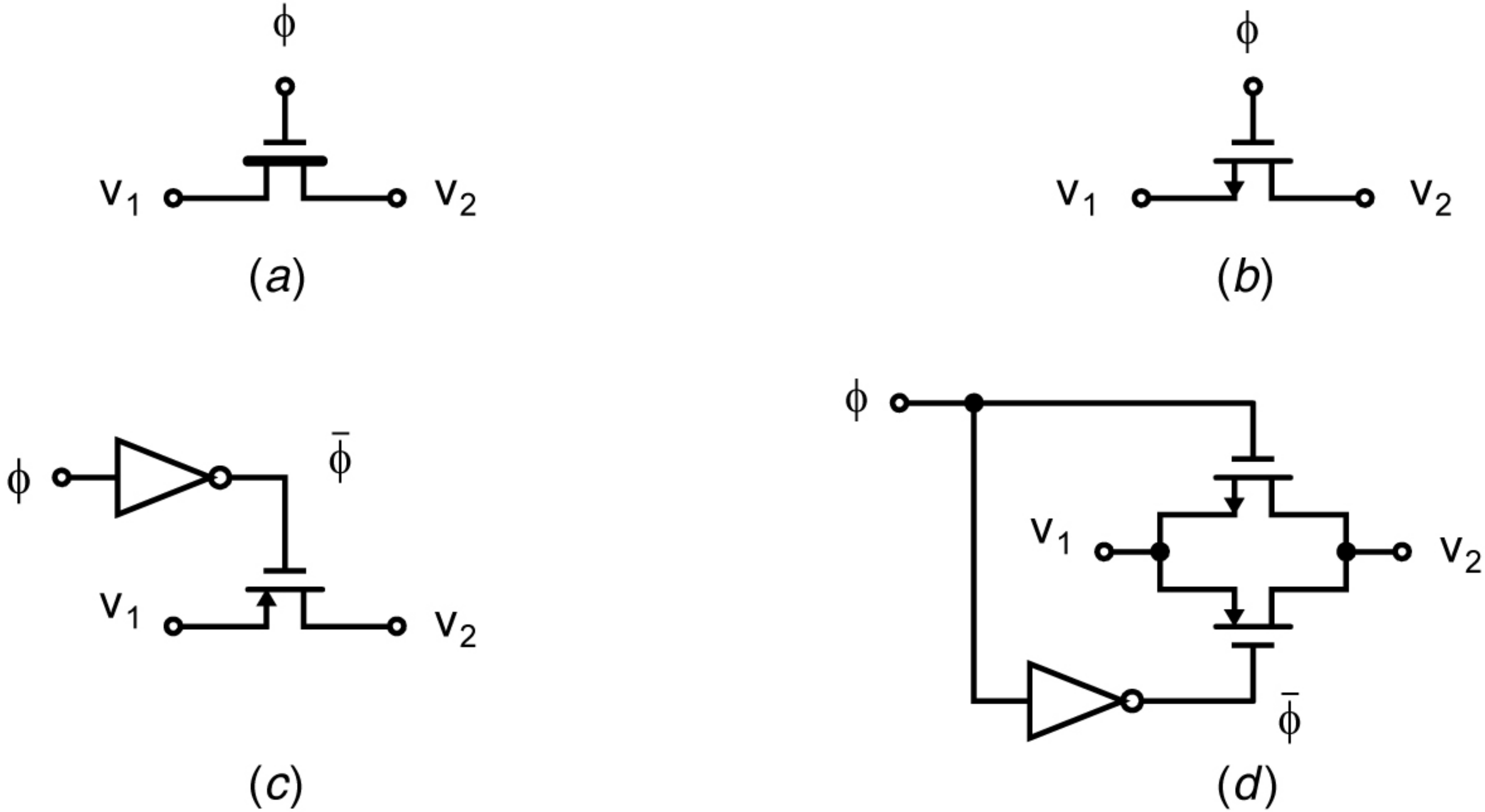
Integrated Circuit Capacitors



Chapter 14 Figure 1

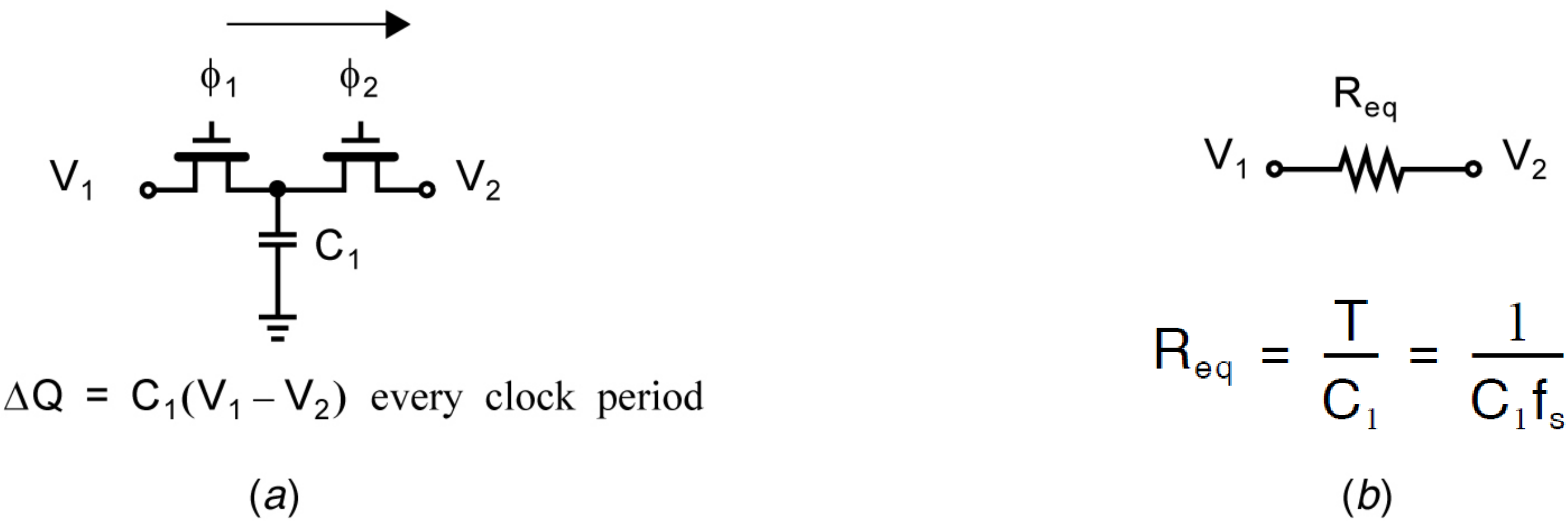
Parasitic capacitances associated with an integrated circuit capacitor are often no symmetric, as indicated by the schematic symbol above

CMOS Switches



Chapter 14 Figure 2: Switch symbol and some transistor circuits: (*a*) symbol, (*b*) n-channel switch, (*c*) p–channel switch, (*d*) transmission gate.

Basic Switched Capacitor

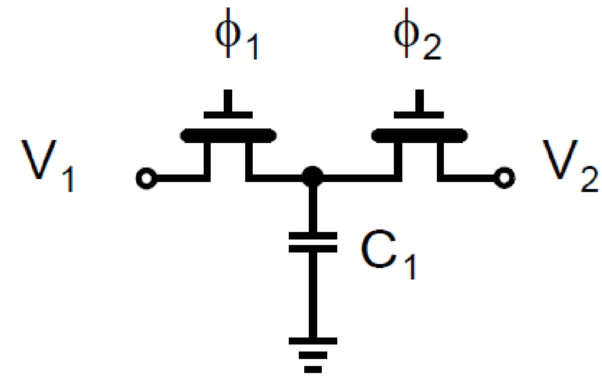


Chapter 14 Figure 4: Resistor equivalence of a switched capacitor. (*a*) Switched-capacitor circuit, and (*b*) resistor equivalent.

Example

- C_1 = 5pF, f_s = 100kHz

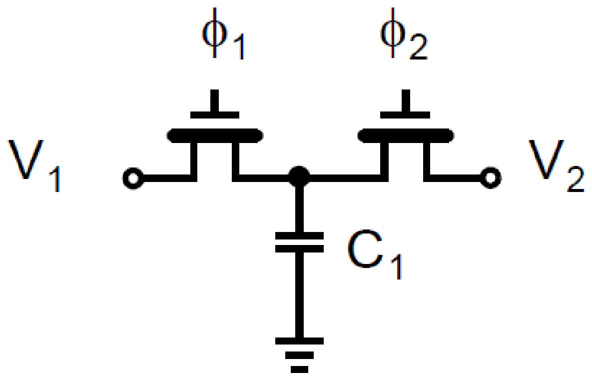
➢ R_{eq} = 1/(5e12*100e3) = 2MΩ!!

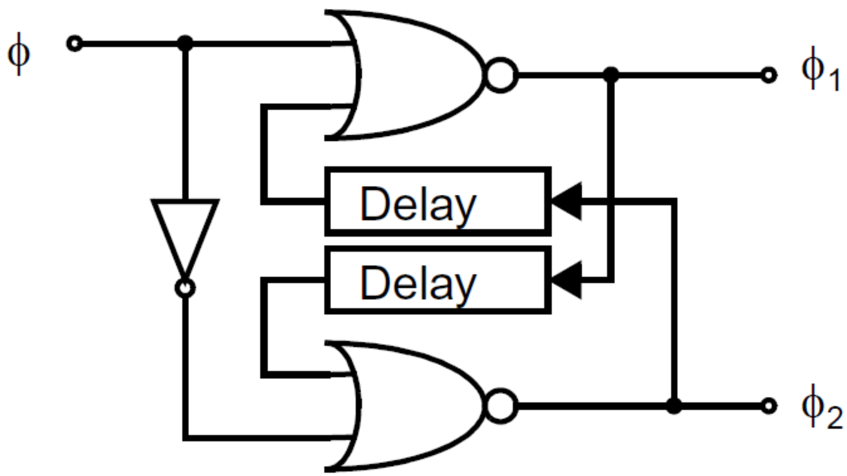


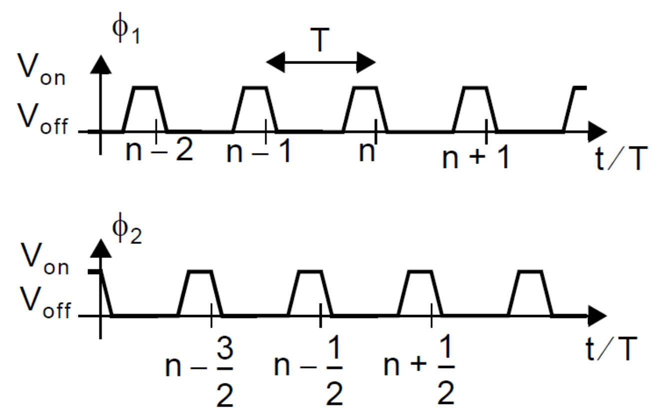
- Very large value
- Controllable by changing the clock frequency

Non-overlapping clocks

- Must avoid the situation where both switches are closed simultaneously

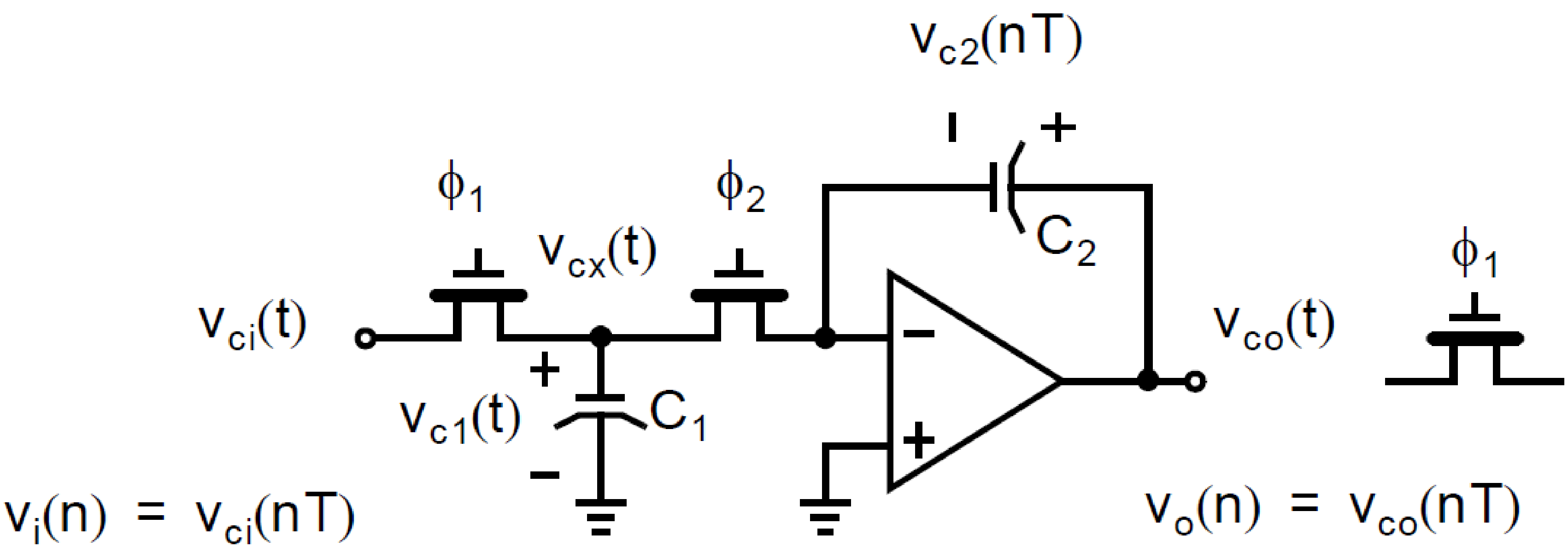


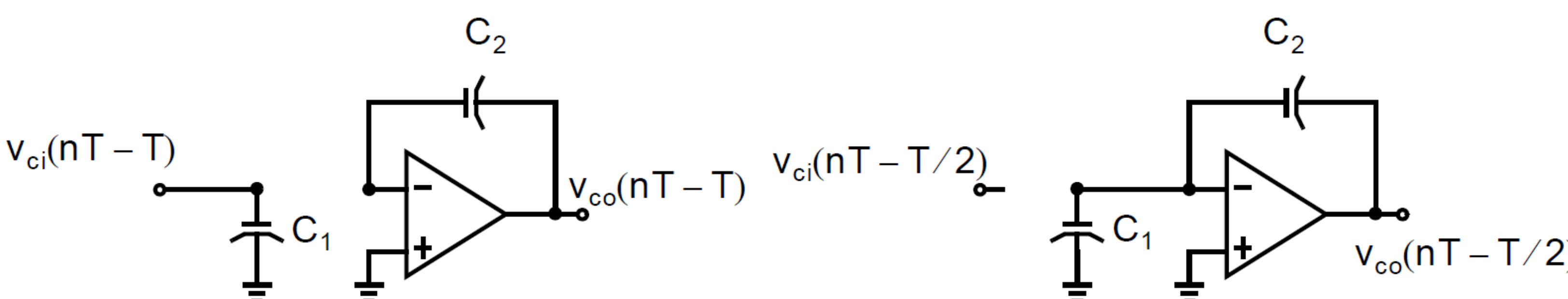




Simple Switched-Capacitor Integrator

(not used)

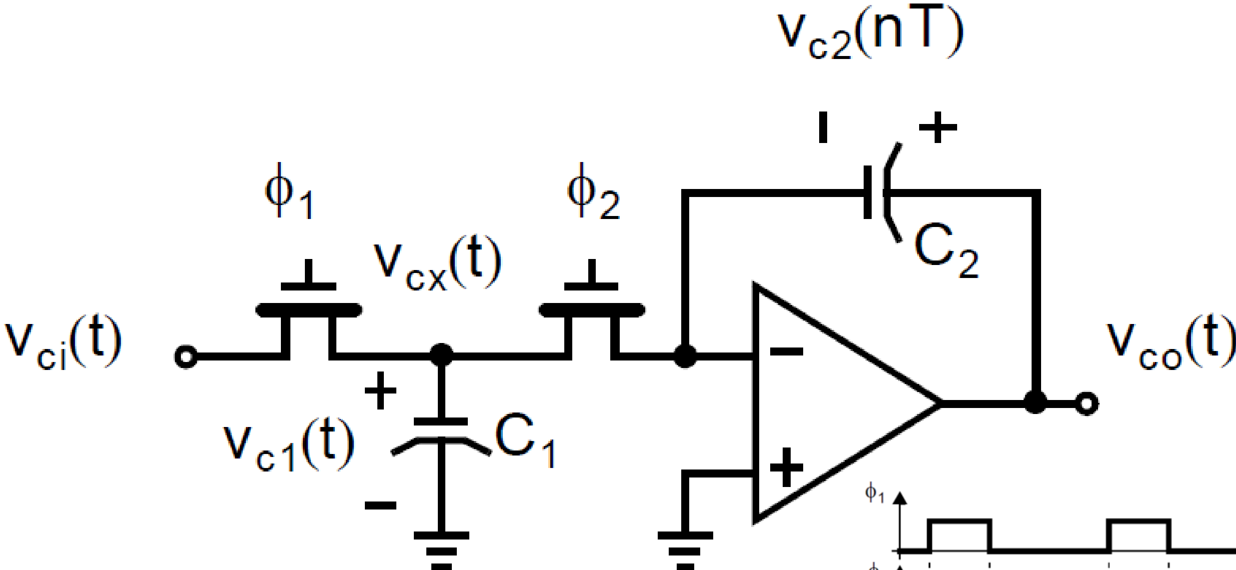


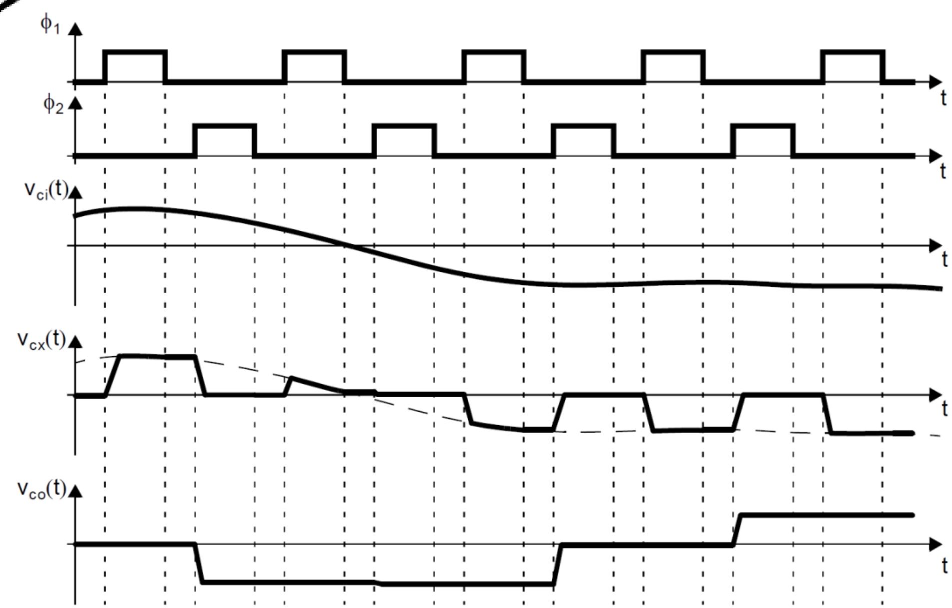


(*a*) (*b*)

Simple Switched-Capacitor Integrator

(not used)





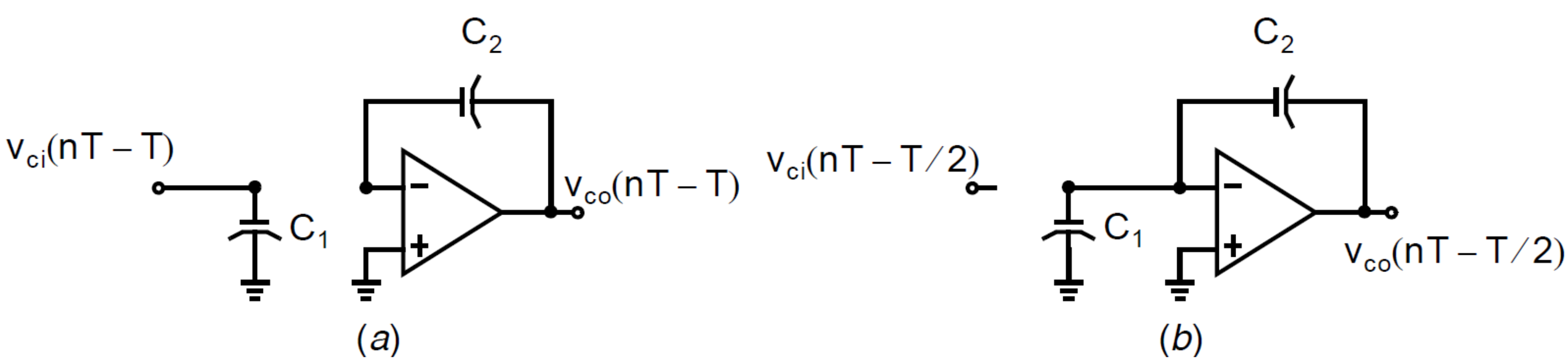
Simple Switched-Capacitor Integrator

(not used)

$$v_o(n) = v_o(n-1) - \frac{C_1}{C_2} v_i(n-1)$$

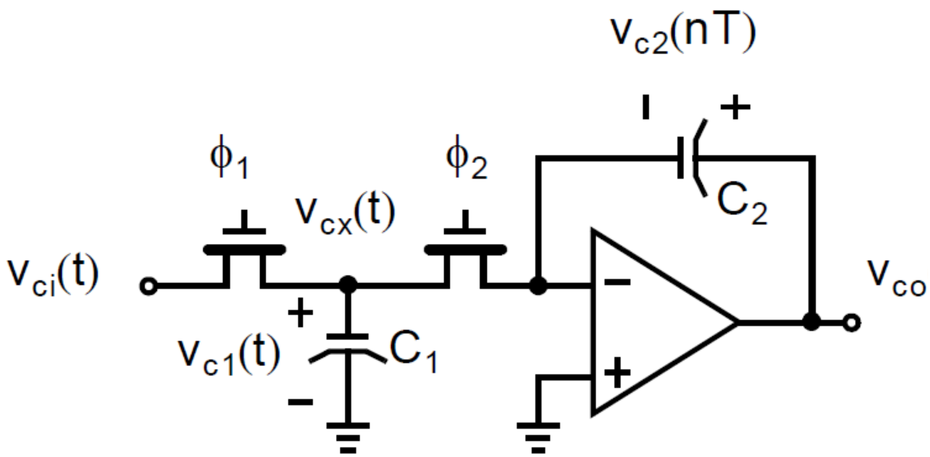
$$V_o(z) = z^{-1} V_o(z) - \frac{C_1}{C_2} z^{-1} V_i(z) \Rightarrow H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right) \frac{z^{-1}}{1 - z^{-1}}$$

$$= -\left(\frac{C_1}{C_2}\right) \frac{1}{z - 1}$$



Simple Switched-Capacitor Integrator

(not used)

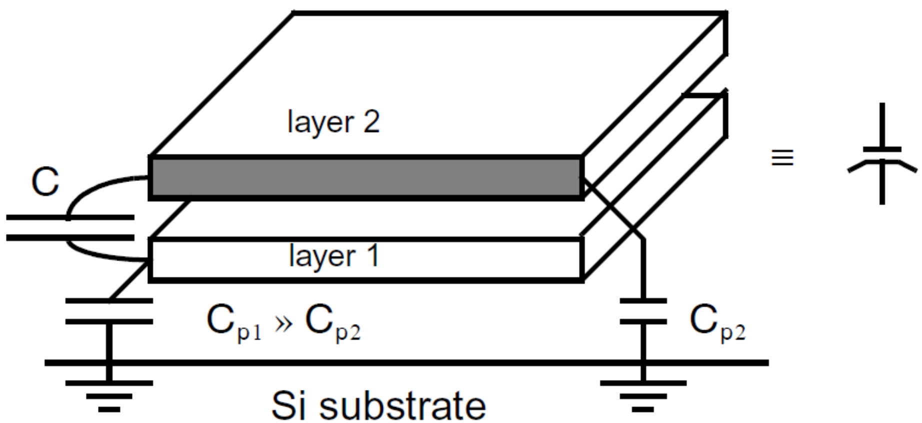


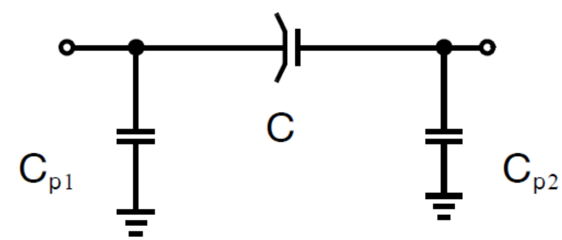
$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right)\frac{z^{-1}}{1-z^{-1}}$$

$$= -\left(\frac{C_1}{C_2}\right)\frac{1}{z-1}$$

- Integrator gain depends upon ratio of capacitor values
- Operation is analogous to a continuous-time active RC integrator with respect to input frequencies >> f_s

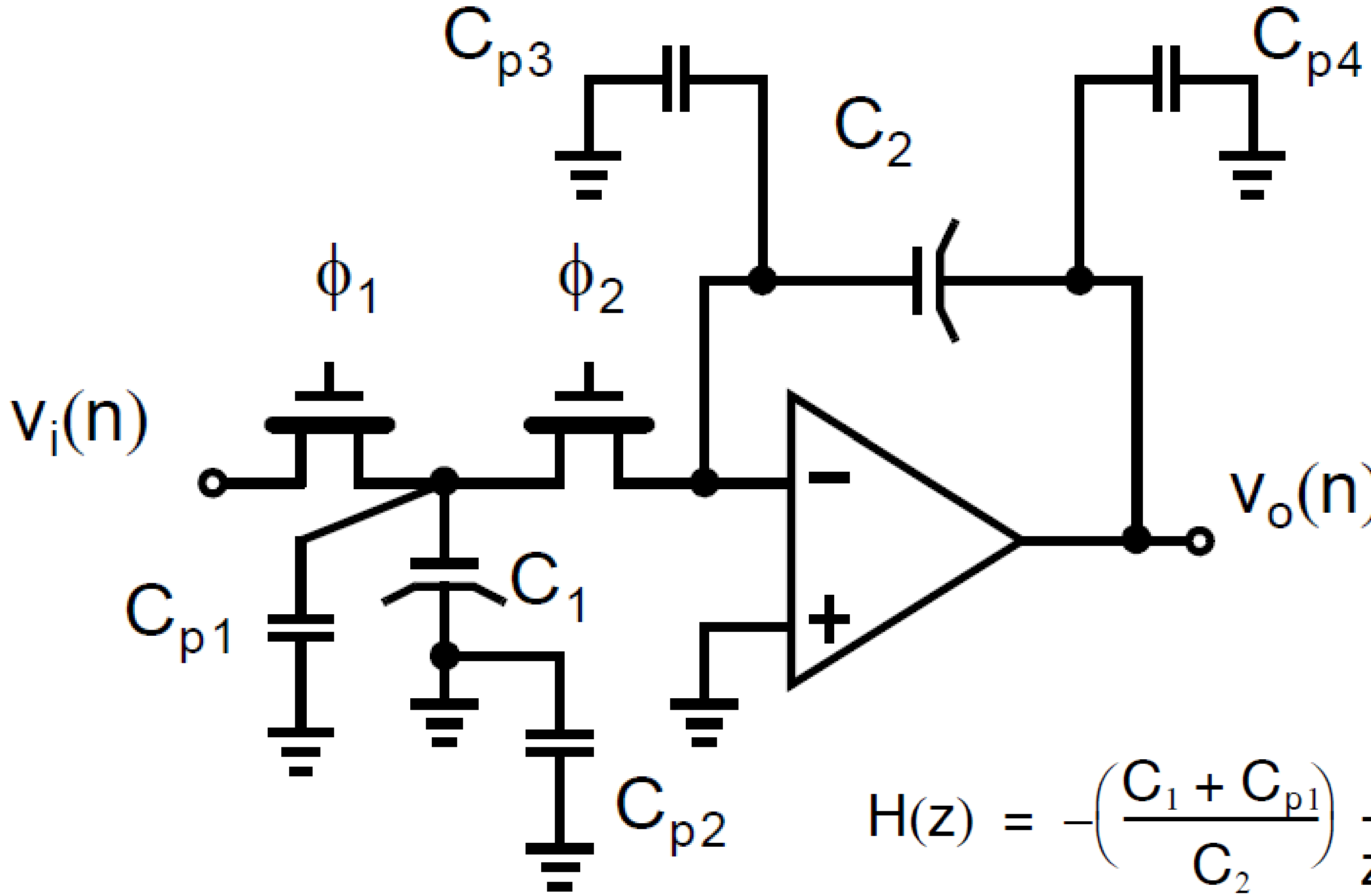
Practical integrated circuit capacitors





- Parasitics $C_{p1,2}$ are not well controlled and are difficult to predict

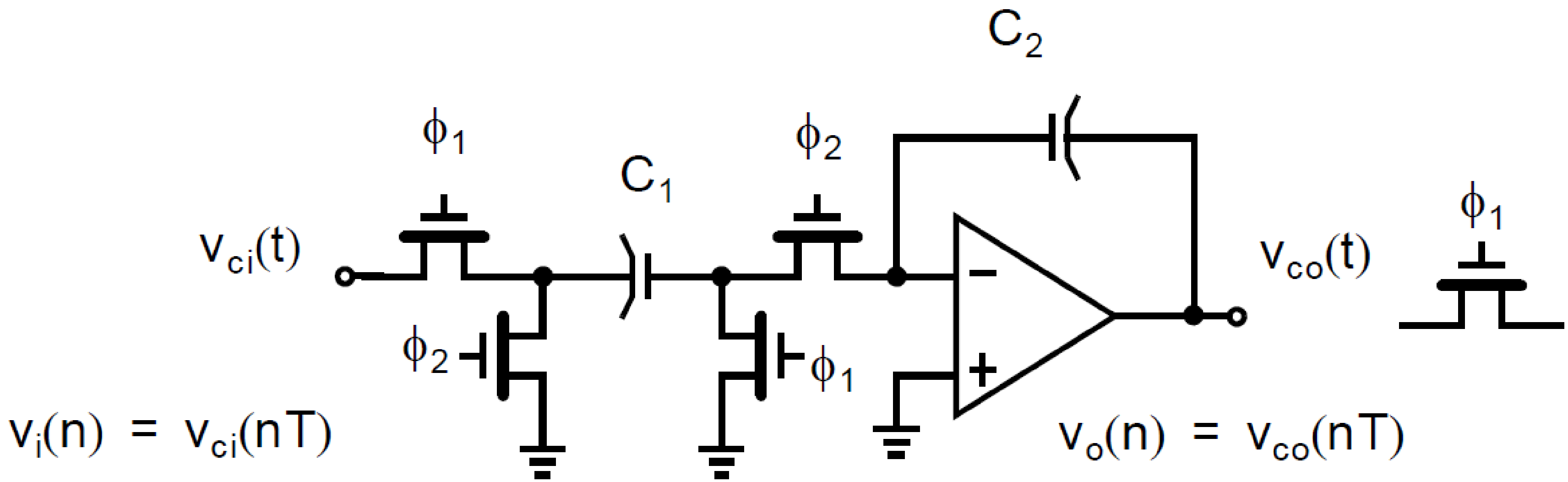
Impact of parasitics on the integrator

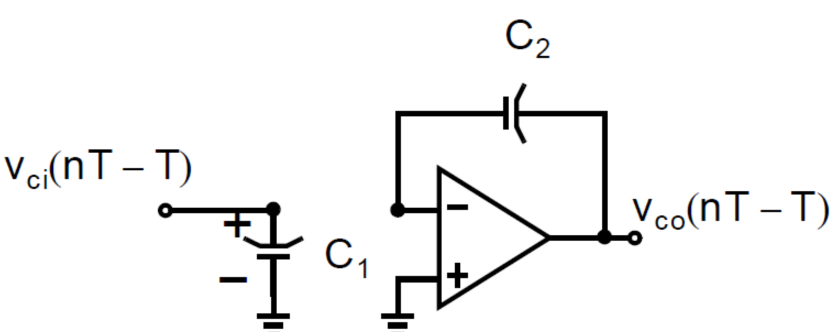


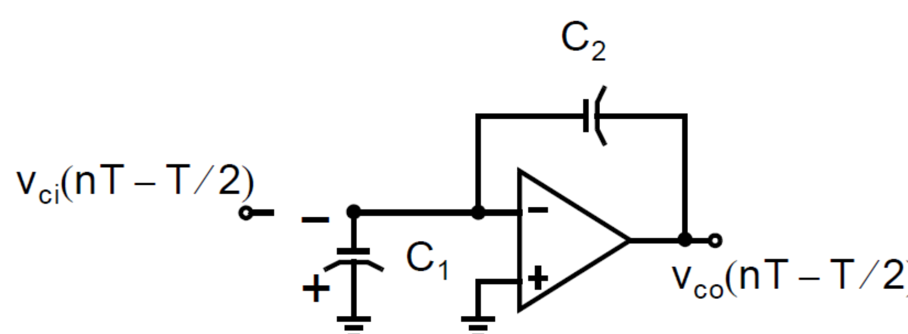
$$H(z) = -\left(\frac{C_1 + C_{p1}}{C_2}\right)\frac{1}{z-1}$$

- Gain is no longer accurate & well controlled

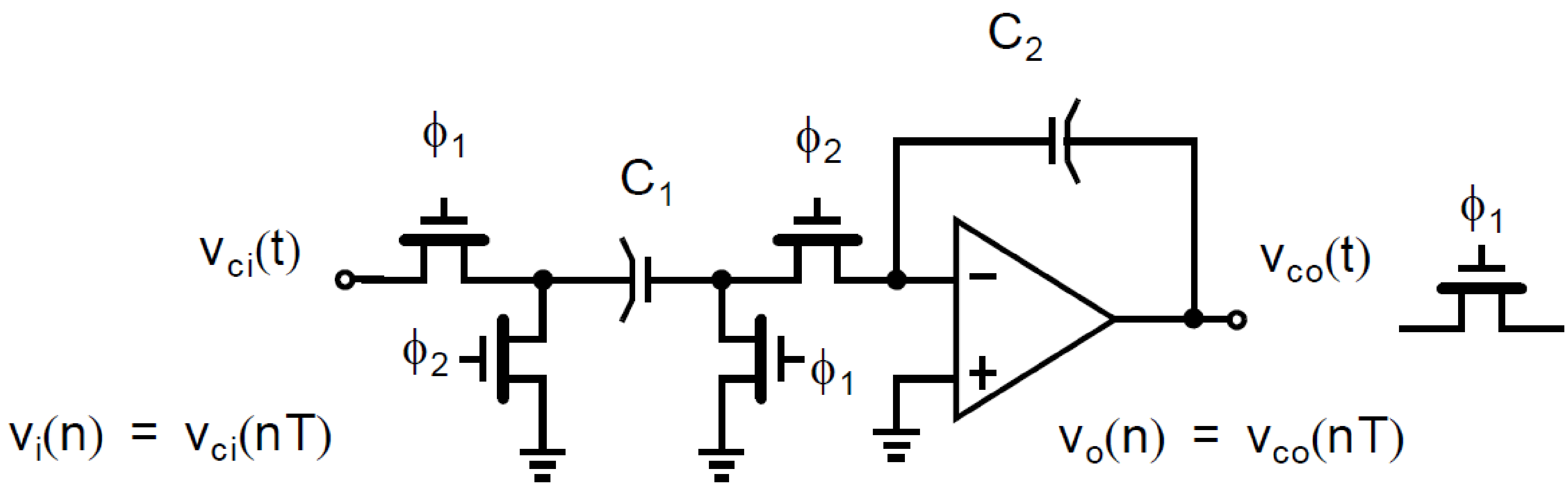
(Noninverting) Delayed Switched-Capacitor Integrator





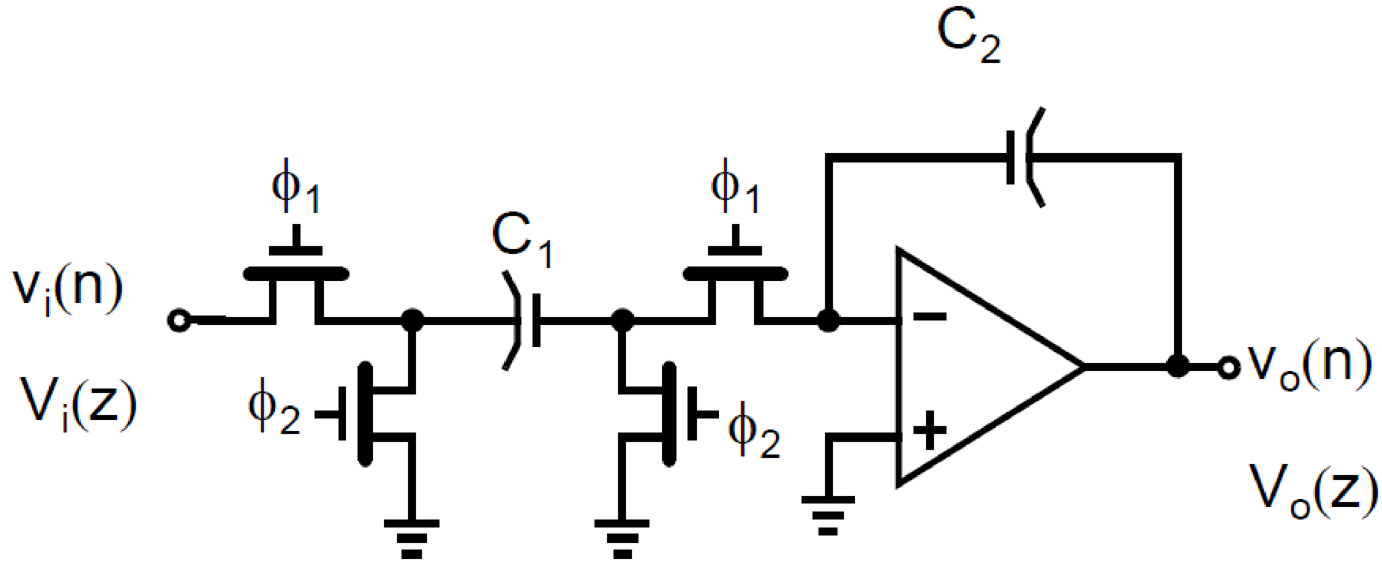


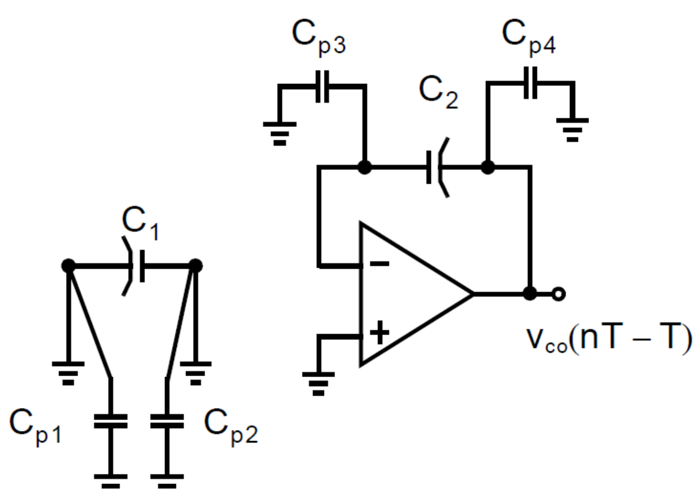
(Noninverting) Delayed Switched-Capacitor Integrator

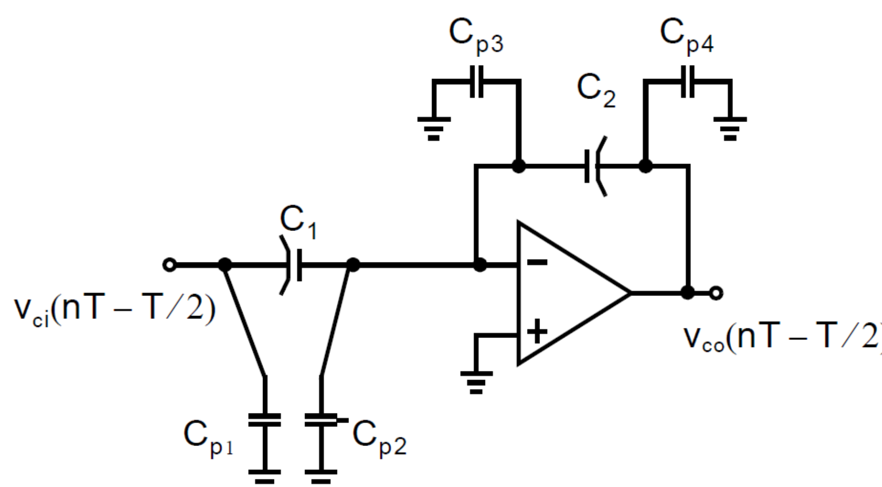


$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = \left(\frac{C_1}{C_2}\right)\frac{z^{-1}}{1-z^{-1}} = \left(\frac{C_1}{C_2}\right)\frac{1}{z-1}$$

(Inverting) Delay-Free Switched-Capacitor Integrator



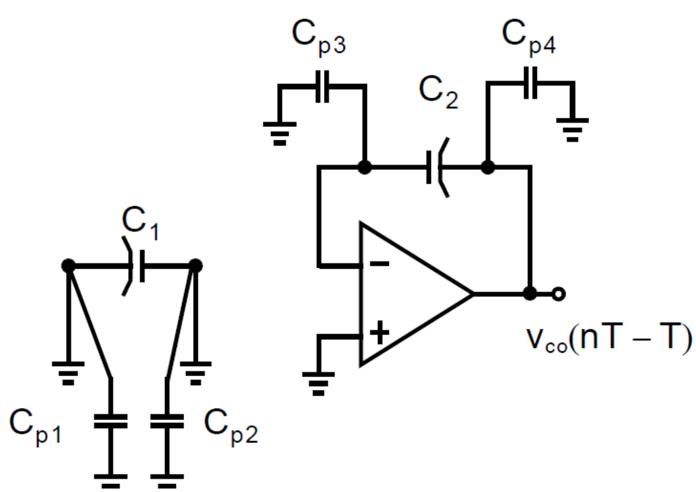


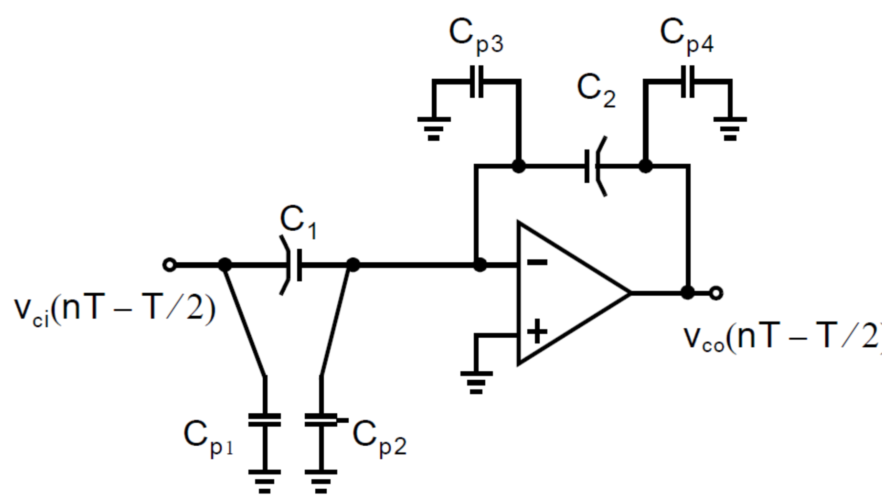


(Inverting) Delay-Free Switched-Capacitor Integrator

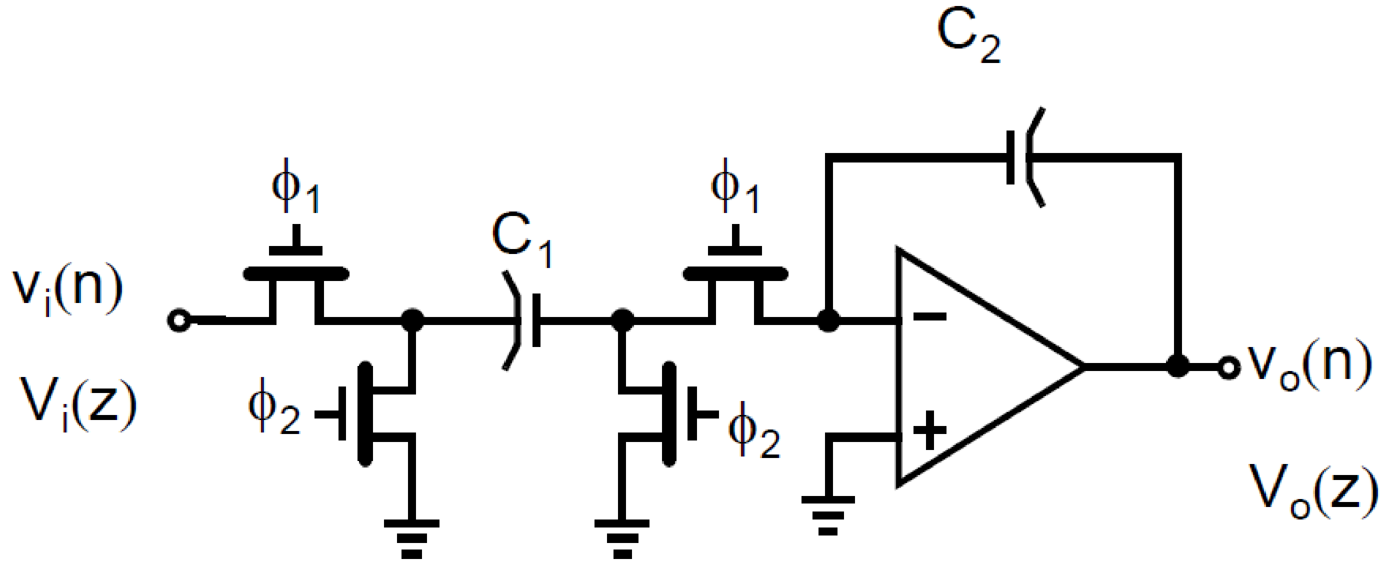
$$C_2 v_{co}(nT) = C_2 v_{co}(nT - T/2) - C_1 v_{ci}(nT)$$

$$v_o(n) = v_o(n-1) - \frac{C_1}{C_2} v_i(n)$$



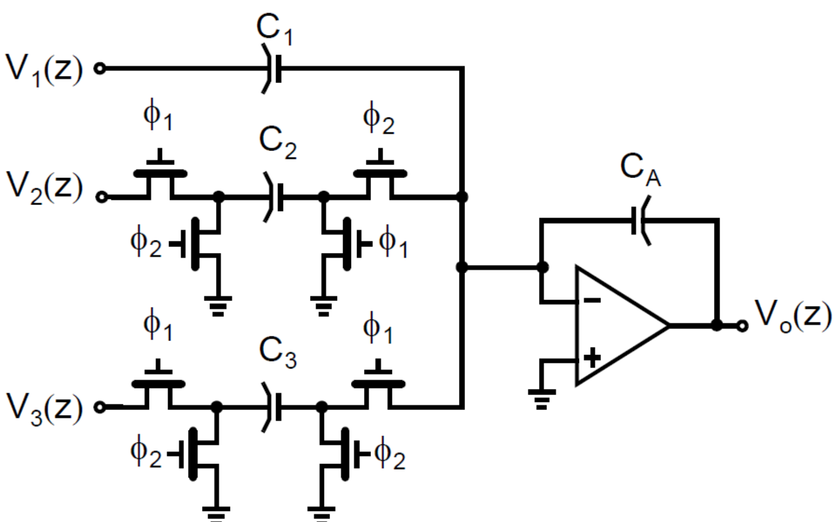


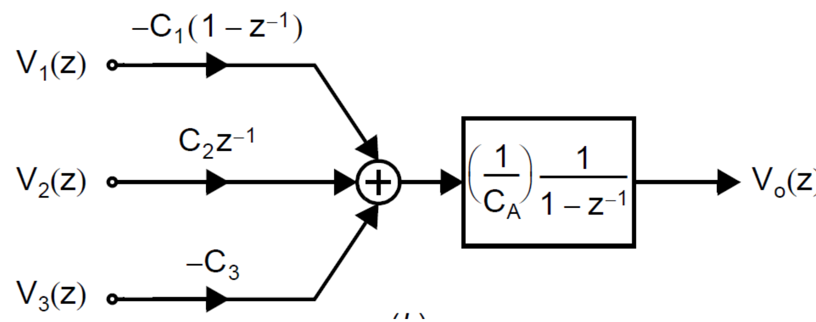
(Inverting) Delay-Free Switched-Capacitor Integrator



$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right)\frac{1}{1-z^{-1}} = -\left(\frac{C_1}{C_2}\right)\frac{z}{z-1}$$

Signal Flow Graph Analysis





$$V_o(z) = -\left(\frac{C_1}{C_A}\right) V_1(z) + \left(\frac{C_2}{C_A}\right)\left(\frac{z^{-1}}{1 - z^{-1}}\right) V_2(z) - \left(\frac{C_3}{C_A}\right)\left(\frac{1}{1 - z^{-1}}\right) V_3(z)$$